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Pyrotransistor - GaAs FET With a "Pyroelectric Wafer" Gate

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Abstract. The multifunction properties of GaAs and other III-V semi-insulating crystals can be expanded by the artificial decreasing of their electric response symmetry that could be transformed from piezo- into a pyroelectric class. An artificial pyroelectricity of III-V type semiconductors can form a basis for one-crystal pyroelectric sensors. The voltage sensitivity of GaAs (111)-cut corresponds to one of PZT pyroelectric ceramics so the GaAs wafer could be used as thermal-to-electric transducer in a new microelectronic device named "pyrotransistor" that is uncooled far infrared detector based on MESFET technology.

Introduction

The current tendency for modern night vision system´s development is the increase of sensor elements number in the receiving matrix (focal plane array). This permits to get rid of optic-mechanical scanning unit and reduces the requirements to sensor element sensitivity because the response is accumulated at all frame duration. The essential feature of such elements is quite uniformity so the sensitivity of each separate elements should differ no more than 0.1% Such uniformity is possible to realize with the application of the modern microelectronic processing. However, far infrared semiconductor sensors use photoconduction and need cooling.

Modern uncooled sensors are based on pyroelectric effect in some polar dielectrics. Pyroelectric ceramics is possible to integrate with semiconductor by microelectronic technology[1]. But the main problem of pyroelectric integrated sensor is to provide negligible thermal contact between pyroelectric transducer and high thermoconductive silicon wafer. So such arrays really need complicated system of packaging. Moreover, the rigid bound of several materials with sharp distinction between their chemical and thermal properties poses problems for technology. For example, as water-soluble pyroelectric-champion TGS so crystals of $LiTaO_3$-type are difficult to integrate with semiconductor matrix processor. Moreover, all pyroelectric cells of such hybrid type "pyroprocessor" have different sensitivity so the effect from this matrix fall short of its ideal.

The possibility exists to use the artificial pyroelectricity in III-V polar semiconductors in order to apply the potentialities of microelectronics for one-crystal thermal imaging[2]. In the proposed case the GaAs-type wafer is a pyroelectric transducer itself while amplifiers and other microelectronics is no more than very thin epitaxial layers with an ultra low thermal mass.

III-V Crystals Polar Properties

Gallium arsenide type crystals, in the first place, are semiconductors and, secondly, they are not pyro- but piezoelectrics. Nevertheless, it will be shown from here on how to get artificial pyroelectric response from piezoelectric of GaAs symmetry.

Piezoelectric and all the more pyroelectric properties of semiconductors have usually been out of consideration because of charge carries screening effect. But in this work ***charge generation process*** is ignored so the term ***charge separation*** [3] has to be used. By this means semiconductor lattice is considered as dielectric and the only electric polarization should be taken into account. This is well represented by semi-insulating GaAs but largely for its solid solutions with AlP.

As a matter of fact, polar properties of GaAs type crystals was taken into account for charge carries mobility and at the sacrifice of this polarity Gunn effect has been supposed. The goal to be sought is to transform the passive i-GaAs wafer into an active thermal-to-electric energy transducer. It is known that only the crystals of pyroelectric symmetry is operable as such transducers while GaAs type crystal are nothing more than piezoelectric.

Pyroelectricity is based on the spontaneous polarization P_s temperature dependence (the primary pyroeffect). The symmetry requires pyroelectric crystal to have unique polar axis which direction coincides with P_s. It is important that pyroelectric coefficient p_i includes also secondary coefficient from piezoelectrically transformed thermal strains. Only 10 from 20 piezoelectric classes of crystals allow pyroelectricity (primary and secondary). Others 10 piezoelectric classes show "latent"polar structure that is self-compensated if crystals are stress-free. But polarity manifests itself over a very wide limits: thermal conductivity of polar crystals is much less than non-polar ones and their thermal expansion coefficient passes through zero at low temperatures (at 60 K for GaAs) instead of showing T^3-dependence). Polar crystal microwave fundamental (lattice) absorption is vastly superior ones of central symmetric crystal and shows the low-temperature maximum of quasi-Debye type. Etching of (111)-GaAs plate depends crucially on "+" and "-" faces just as in pyroelectric crystals. At last, the growing GaAs crystal can swim in its melt just as the ice in the water because the arrangement of crystal polar bonds expands the material.

Recently it has been originally shown that uniform thermal influence induces pyroelectric response in all 20 piezoelectric classes of crystals if they are partially clamped [4]. In the case being considered the GaAs unit cell posseses an octupole-type latent polarity which has to be totally compensated because of its four 3-fold polar axes are crossing at angle of 109.5°. But the self-compensation could be artificially broken due to a partial limitation of strains under the special boundary conditions.

Thermomechanically induced response

Thin GaAs crystal plate of (111)-cut shows a longitudinal piezoeffect $P_3 = e_{33} x_3$ where "3" is [111]-axis and transverse piezoeffect $P_3 =$ $= (e_{31}+e_{32})x_3$. The sum of piezoelectric coefficients $e_{31}+ e_{32}+e_{33} = 0$ so any scalar influence totally compensates each other if crystal is

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free to expand. This compensation is shown on Fig.1b for GaAs crystal thermal treatment: piezoelectric contribution from the longitudinal strain component $x_3 = \alpha\,dT$ is compensated by two transverse components $x_1 = x_2 = \alpha\,dT$. If the last ones are forbidden by planar clamping the polarization $P_3 = e_{33}\cdot\alpha\cdot dT$ will imitate "pyroelectricity" (α is thermal expansion coefficient). So the used effect is equivalent to the secondary pyroelectric effect that is inherent to pyroelectrics but previously unknown in piezoelectrics.

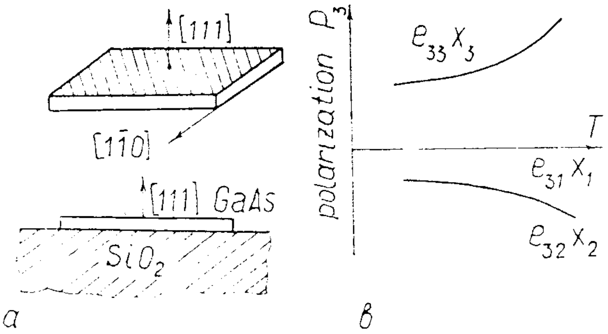

Fig.1. Thermal treatment of semi-insulating GaAs thin plate cemented on silica (a); thermal strains produce polarization (b).

Any variation of P_3 with the temperature produces in GaAs artificial pyrocoefficient:

$$p_3 = dP/dt = 2\sqrt{3}\, d_{14}\, \alpha\,/(4\,S_{11} + 8S_{12} + S_{44}),$$

where d_{14} is piezoelectric constant and S_{mn} is elastic compliance. It is evident that (111)-cut shows a maximum of effect. The angle dependence of p in the spherical coordinates is:

$$p\ (\theta,\varphi) = p_3 \sin 2\theta \sin \theta \sin 2\varphi$$

where θ is the angle deflection from [111] = 3 axis and φ is azimuth.

In our "static" experiments thin GaAs plate was cemented to hard substrate (fused silica in Fig.1a) with low thermal expansion coefficient. This is convenient for performing measurements but for device application the finned structure (produced by special etching) is sufficient to provide planar strains limitation. For the same purpose wafer-transducer could be compressed in its plane bounded by a rigid ring. In any case, only thermally induced thickness strain should be permitted and just in the direction of [111] type polar axis.

It was obtained that GaAs "pyrocoefficient" is 1.5·10 µC/m²K with the voltage sensitivity $S_v = 0.02\ m^2C^{-1}$. Our investigations show that some of III-V semiconductors that is capable to form solid solutions with GaAs have these parameters 10 times more. Above all, they are much closer to dielectrics than semi-insulating GaAs.

Construction of Pyrotransistor

GaAs type artificial "pyrotransducer" integrated with FET amplifier can be basis of a new microelectronic device named "pyrotransistor". The last one consists of MESFET with submicron channel that can be realized out of thin epitaxial layer deposited onto (111)-cut wafer operating as a "pyrogate".

Infrared radiation could be absorbed as by a special IR-absorbent covering the back side of wafer so due to internal IR absorption of wafer (that could be explained by III-V crystal pol lattice and by its imperfections and doping).

The first method is usually used in the py roelectric detectors based on the ferroelectr materials with the very high IR reflection a large near-surface IR absorption. Thermal di fusion from IR-absorbent to pyroelectric boun operation speed. As applied to semi-insulati GaAs, the modulating frequency about 1 KHz required at which the temperature wave leng in GaAs wafer is about 100 µm. The more thi wafer could not essentially increase the "pyr electric" response.

The occasion of internal absorption seems t be more interesting because it is inherent t the III-V type crystals only that are sem transparent for infrared radiation. Thermal-to electric response could be got directly in th crystal lattice without any delay while MESF is also capable to rapid operation with puls rise about 10^{-11}c. So the inertialess is one the advantages of new device.

In GaAs and related crystals the absorpti and transparency may be "resonant" in the rang over 8-14 microns but an enlightenment layer desirable in order to decrease IR reflectio Fig.2 shows the reflection coefficient for t 100 µm wafer thickness near 10 µm wavelengt as a function of GaAs dielectric absorption K" The last depends on doping and can be controlled. At increased absorption the IR reflecti is rather small but the only close-to-surfa part of the wafer can work as transducer.In t opposite case IR radiation is absorbed in al bulk wafer while the reflection gains resona character, Fig.2. The reflection coefficie passes trough minimum and increases thereafte The device with internal absorption could applied for a very fast IR pulses measureme

Modulation frequency of IR-radiation in th III-V crystal"pyrodetector" depends on the equilibrium concentration of charge carries.In th standard (10^{-8} Ohm^{-1}m^{-1}conductivity) semi-insulating GaAs the screening of pyroelectric fiel is overlooked at the modulation frequency 1 KH In some GaAs -III-V solid solutions this frequency would be reduced to 20 Hz.

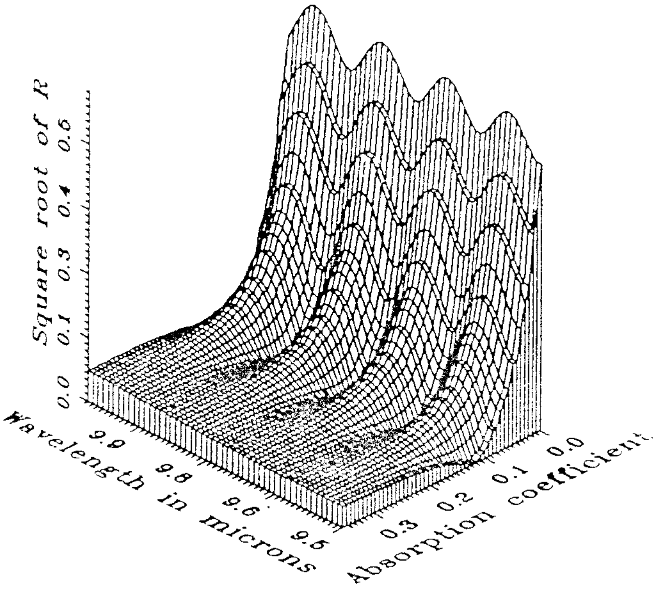

Fig.2 IR reflection coefficient modulus versu IR wavelength and GaAs crystal absorption coefficient (K" is the imaging part of complex dielectric permittivity).

The MESFET discussed below contains a high-level doped epitaxial layer deposited onto semi-insulated wafer=substrate, Fig.3. The submicron MESFET conducting channel is located near the boundary: epitaxial layer - substrate that is in the vicinity of potential energy minimum. The last is formed by the back-biased Schottky barrier and by the contact potential barrier from substrate. The response Ep is capable to change the potential barrier height and shape.

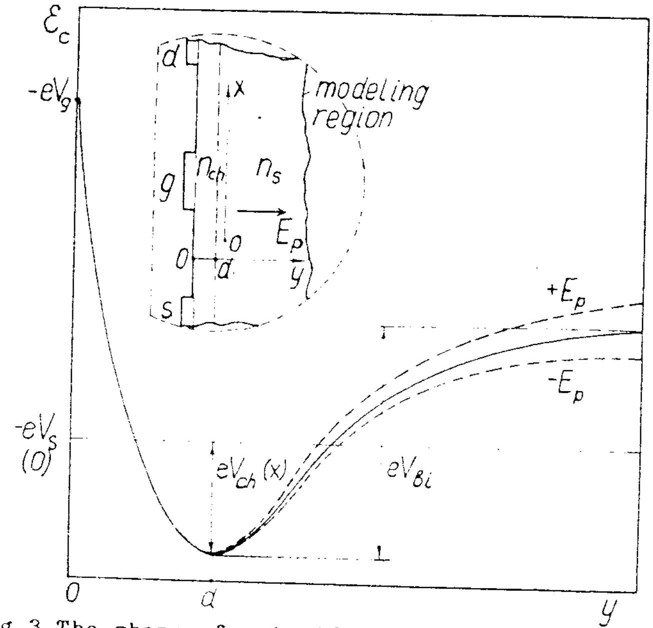

Fig.3. The shape of potential in the under-gate vicinity of channel: s - sourse, g - gate, d - epitaxial layer thickness, Ep - pyro-electric field.

Produced by the charge carries diffusion into semi-insulating substrate from channel, the enrichment layer plays a crucial role in source-drain (S-D) conductivity if the channel length is less then 1um. It is in short channel MESFET where S-D conductivity is strongly dependent on substrate potential due to the variations of the enrichment layer thickness. The last could be controlled by the wafer internal electric field Ep. Moreover, this field changes channel length that in its turn also controls a MESFET drain current.

Quasi two dimensional kinetic model [5] and the Monte-Carlo method [6] were used for MESFET pyrotransistor simulation. In the course of modelling of short-channel structure the main peculiarities of submicron device were accounted. Those are: drift speed overshoot, the substrate shunting influence and electrogradient effects. Some processes in the interface layer are also connected with the injection of charge carriers and their redistribution between channel and substrate. Simulation predicts that realization of submicron field structure pyrotransistor is possible with following main parameters: 0.5 um distance between drain and source electrodes; 0.2 x 500 µm gate size; 0.06 µm thickness of epitaxial layer that has 4 10^{17} cm^{-3} doping level; 100 um thickness of substrate=wafer with a 2 10^{14} cm^{-3} doping level. This structure is possible to arrange over 50 x 50 µm² crystal area in a meander type design. Simulations show the most profitable drain current control could be got near the threshold region of MESFET characteristics (if the gate potential is close to the pinch-off voltage). This mode of operation provides also the least noise factor of MESFET.

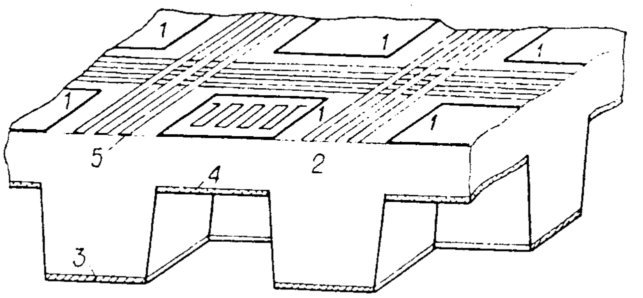

Fig.4. Detector cell in the crystal array:
1 - schematized MESFET, 2 - substrate (wafer), 3 - metallized ridges, 4 - absorbent layer in the valley, 5 - readout circuits.

As a result the wafer heating on 0.1 K leads to drain current change in 40 µA at gate potential Vg = 0 V. At the gate potential Vg = -1 V the change of drain current is 50 µA.

Fig.4 shows the topology of "single cell-element" and its environment in form of valleys and ridges. Produced by the etching, a stepwise back-face of wafer is required to the partial clamping realization. The finned design provides IR reflection from metallized ridges and practically full absorption of valleys covered by IR-absorbent layer or by enlightenment layer if the wafer absorption is intrinsic. Each valley is an under-MESFET "pyroelectric" region.

Conclusion

Planar strain limitation in the [111]-cut of III-V type of semi-insulating crystals opens up possibilities for new type of microelectronic sensor that is uncooled and one-crystal array. The last has advantages as over semiconductor photonic arrays that need cooling so over pyroelectric ones produced by hybrid processing.

Hundreds of pyrotransistors on the same wafer would form matrix thermal image processor which sensitivity increases as square root from cells number. The current status of microelectronics can guarantee the identity of each cell in this one-crystal.

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